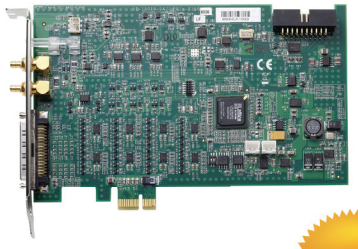
PCIe-7350

50 MHz 32-CH High-Speed Digital I/O Card

PCI EXPRESS®



NEW

Features

- x1 lane PCI Express® Interface
- Maximum 50 MHz clock rate from internal timer or 100 MHz from external clock
- 200 MB/s maximum throughput
- Software selectable voltage level of 1.8 V, 2.5 V, and 3.3 V
- 16-steps phase shift in external clock mode
- Per group (8-bit) input/output direction selectable
- Supports I²C and SPI programmable serial interfaces for external device communication
- Scatter-gather DMA support
- Flexible handshaking and external digital trigger modes
- 8-channel auxiliary programmable I/O

Operating Systems

• Windows Vista/XP/2000/2003

Recommended Software

• VB.NET/VC.NET/VB/VC++/BCB/Delphi

• DAQBench

Driver Support

• PCIS-DASK for Windows

Introduction

ADLINK's PCIe-7350 is a high-speed digital I/O board with 32-channel bi-direction parallel I/O lines. The data rate can achieve up to 200 MB/s through the x1 PCI Express® interface. The clock rate can support up to 50 MHz internal clock or 100 MHz external clock, which is ideal for the applications of high-speed and large-scale digital data acquisition or exchange, such as digital image capture, video playback and IC testing.

I/O Port Configuration & Level Shifting

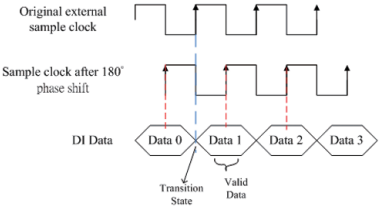
The PCIe-7350's initial status (power-up status) of the on-board 32-channel I/O lines is preset as input lines. The 32-channel I/O lines are bi-direction and can be divided into four groups. Each group contains 8 channels and can be individually configured as an input or output port. The PCIe-7350 also supports software selectable logic level of 1.8 V, 2.5 V, and 3.3 V. When you select one of the logic levels, all the four groups will be at the same logic level you choose. In digital output mode, the outputs are tri-stated when the digital output lines are disabled. The programmable I/O direction and logic levels provide a flexible interface to the device under test (DUT).

Maximum Data Transfer Rate

The PCIe-7350 can support a maximum of 200 MB/s throughput along with a 32-bit data width at a maximum 50 MHz internal clock rate or 8/16-bit data width at a maximum 100 MHz external clock rate. The combination scatter-gather bus-mastering DMA, deep on-board 8 k-sample FIFO size, and x1 PCI Express® interface guarantee no data loss during sustained high-speed data processing.

Phase Delay

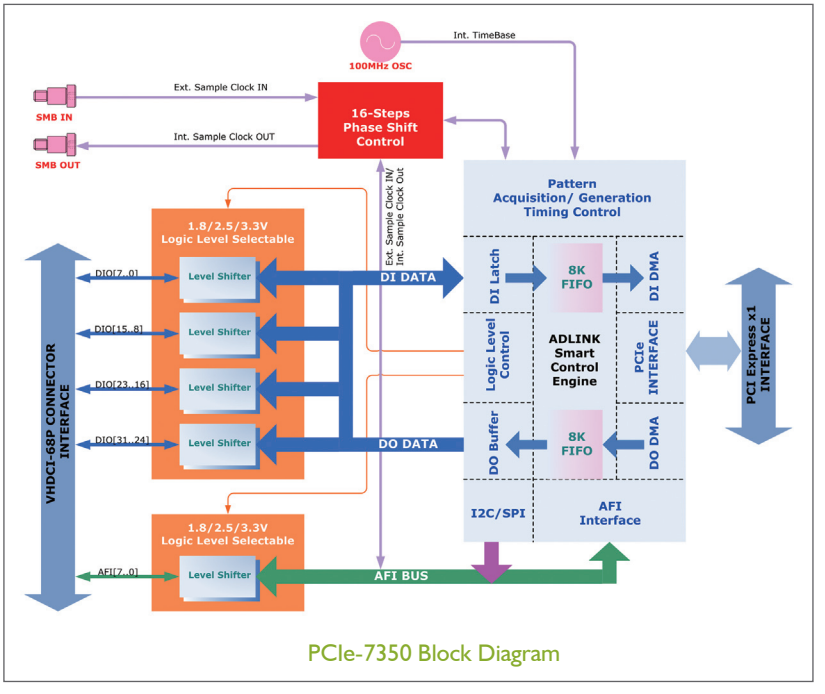
The PCIe-7350 features phase shifting of external sample clock or internal sample clock exporting, which allow you to optimize the acquisition/generation timing in high-speed data transfer applications. The phase shifting of sample clock is capable of up to 16-steps adjustment– that is, the phase shifting can be adjusted from 22.5 degrees to 337.5 degrees. This feature thus prevents sampling at the transition state of the acquired data to ensure sample timing is valid and in stable condition. The left timing diagram is the examples of 180-degree phase shift for digital data acquisition and generation.



External Clock @ Rising edge Sampling --- 180-degree phase shift

I²C & SPI Serial Interfaces

PCIe-7350's application function I/O (AFI) can be configured as a I²C or SPI master node. The I²C interface supports fast mode and uses two bi-direction lines called SCL (serial clock) and SDA (serial data). The SPI interface uses three-wire signaling called SCK (serial clock), SI (serial data input), and SO (serial data output). Communication with peripheral devices can be directly performed through the PCIe-7350's built-in I²C or SPI protocols along with provided APIs.



PCIe-7350 Block Diagram

Specifications

Digital I/O

- Number of channels:
  32, per group (8-channel) input/output direction selectable logic levels: 1.8 V, 2.5 V, 3.3 V (software selectable)
- Power-up status: All digital inputs
- Impedance:
  • Input: 10 kΩ
  • Output: 50 Ω
- Input protection: -1 to 6 V
- Data transfer: Programmable I/O, bus-mastering DMA with scatter-gather
- Maximum data transfer rate: 200 MB/s
- Digital logic levels:

Logic Levels		1.8 V	2.5 V	3.3 V
Digital Input	Min. input high voltage	1.2 V	1.6 V	2 V
	Max. input low voltage	0.63 V	0.7 V	0.8 V
Digital Output	Min. output high voltage	1.6 V	2.3 V	3.1 V
	Max. output low voltage	0.2 V	0.2 V	0.2 V
	Max. output driving current	8 mA	16 mA	32 mA

Clocking mode

- Internal clock: Max. 50 MHz (100 MHz / N; 2<N<65535)
- External clock: Max. 100 MHz (support 8/16-bit data width only, data throughput must be less than 200 MB/s)
- Handshaking
- Burst handshaking

Trigger sources

- Software trigger
- External digital trigger: AFI[0…7]

Trigger modes

- Post trigger, Retrigger, Pattern match, Handshaking

Change of State Interrupt

- Interrupt sources: Any of 32 channels or a pre-define channel Change-of-State

Application Function I/O

- Number of channels: 8
- Supporting modes: static I/O, I^2C or SPI master node, external clock input/output, external digital trigger input, handshaking

Cable & Terminal Boards

- DIN-68H-01
  Terminal Board with One 68-pin SCSI-VHDCI Connector and 0 or 50 Ω Jumper Selectable Impedance (cables not included)
- ACL-10279
  • 68-pin SCSI-VHDCI Cable with 50 Ω Impedance
- SMB-SMB-1M
  • SMB to SMB Cable, 1M

Ordering Information

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  50 MHz 32-CH High-Speed Digital I/O PCI Express® Card
- **DIN-68H-01**
  Terminal Board with One 68-pin SCSI-VHDCI Connector and 0 or 50 Ω Selectable Impedance


ACL-10279


SMB-SMB-1M


DIN-68H

Pin Assignment

GND	68	34	GND
AFI7(DI CLK)	67	33	AFI6 (DO CLK)
GND	66	32	GND
D0	65	31	D1
AFI5	64	30	AFI4
D2	63	29	D3
GND	62	28	GND
D4	61	27	D5
AFI3	60	26	AFI2
D6	59	25	D7
GND	58	24	GND
D8	57	23	D9
GND	56	22	GND
D10	55	21	D11
GND	54	20	GND
D12	53	19	D13
AFI1	52	18	GND
D14	51	17	D15
GND	50	16	GND
D16	49	15	D17
GND	48	14	GND
D18	47	13	D19
GND	46	12	GND
D20	45	11	D21
GND	44	10	GND
D22	43	9	D23
GND	42	8	AFI0
D24	41	7	D25
GND	40	6	GND
D26	39	5	D27
GND	38	4	GND
D28	37	3	D29
GND	36	2	GND
D30	35	1	D31