Quick Selection Guide

Model number	Analog Input				Analog Output			DIO	Timer/Counter
	No. of channels	Resolution	Sampling rate	Input range	No. of channels	Resolution	Update rate	No. of channels	No. of channels
PXI-2204	32DI/64SE	12 bits	3 MS/s	±0.05 V to ±10 V	2	12 bits	1 MS/s	24-CH 8255 PIO	2-CH, 16-bit
PXI-2205	32DI/64SE	16 bits	500 kS/s	±1.25 V to ±10 V	2	12 bits	1 MS/s	24-CH 8255 PIO	2-CH, 16-bit
PXI-2206	32DI/64SE	16 bits	250 kS/s	±1.25 V to ±10 V	2	12 bits	1 MS/s	24-CH 8255 PIO	2-CH, 16-bit

Specifications

Model Number	PXI-2204	PXI-2205	PXI-2206
Analog Input			
Resolution	12 bits, no missing codes	16 bits, no missing codes	16 bits, no missing codes
Number of channels	64 single-ended or 32 differential (software selectable per channel)		
Channel gain queue size	512		
Maximum sampling rate	3 MS/s	500 kS/s	250 kS/s
Programmable gain	1, 2, 4, 5, 8, 10, 20, 40, 50, 200	1,2,4,8	1,2,4,8
Bipolar input ranges	±10 V, ±5 V, ±2.5 V, ±1.25 V, ±1 V, ±0.5 V, ±0.25 V, ±0.2 V, ±0.05 V	±10 V, ±5 V, ±2.5 V, ±1.25 V	±10 V, ±5 V, ±2.5 V, ±1.25 V
Unipolar input ranges	0-10 V, 0-5 V, 0-4 V, 0-2.5 V, 0-2 V, 0-1 V, 0-0.5 V, 0-0.4 V, 0-0.1 V	0-10 V, 0-5 V, 0-2.5 V, 0-1.25 V,	0-10 V, 0-5 V, 0-2.5 V, 0-1.25 V
Offset error	±1 mV	±1 mV	±1 mV
Gain error	±0.03% of FSR	±0.01% of FSR	±0.01% of FSR
Input coupling	DC		
Overvoltage protection	Power on: continuous ±30 V, Power off: continuous ±15 V		
Input impedance	1 GΩ/100 pF		
CMRR (gain = 1)	90 dB	83 dB	83 dB
Settling time	1 μs to 0.1% error *	2 μs to 0.1% error	4 μs to 0.01% error
-3dB small signal bandwidth (gain = 1)	2 MHz	1.6 MHz	760 kHz
Trigger sources	Software, external digital/analog trigger, and PXI trigger bus		
Trigger modes	Pre-trigger, post-trigger, middle-trigger, delay-trigger, and repeated trigger		
FIFO buffer size	1 k samples		
Data transfers	Polling, scatter-gather DMA		
Analog Output			
Number of channels	2 voltage outputs		
Resolution	12 bits		
Output ranges	0-10 V, ±10 V, 0-AOEXTREF, ±AOEXTREF		
Maximum update rate	1 μs		
Slew rate	20 V/μs		
Settling time	3 μs to ±0.5 LSB accuracy		
Offset error	±1 mV		
Gain error	±0.02 % of max. output		
Driving capacity	±5 mA		
Stability	Any passive load, up to 1500 pF		
Trigger sources	Software, external digital/analog trigger, PXI trigger bus		
Trigger modes	Post-trigger, delay-trigger, and repeated trigger		
FIFO buffer size	1 k samples		
Data transfers	Programmed I/O, scatter-gather DMA		
Digital I/O			
Number of channels	24-CH 8255 programmable input/output		
Compatibility	5 V/TTL		
Data transfers	Programmed I/O		
General-Purpose Timer/Counter			
Number of channels	2		
Resolution	16 bit		
Compatibility	5 V/TTL		
Base clock available	40 MHz, external clock up to 10 MHz		
Auto Calibration			
On-board reference	+5 V		
Temperature drift	±2 ppm/°C		
Stability	±6 ppm/1000 Hrs		
General Specifications			
Dimensions	160 mm x 100 mm (not including connectors)		
Connector	68-pin VHDCI female x 2		
Operating temperature	0 to 55 °C		
Storage temperature	-20 to 80 °C		
Humidity	5 to 95 %, noncondensing		
Power requirements	+5 V 1.3 A typical	+5 V 1.2 A typical	+5 V 1.2 A typical

*Gain = 1, 2, 4, 8

* All specifications are subject to change without further notice.