PCI-7300A

80 MB/s High Speed 32-CH Digital I/O Card

Features

- Supports a 32-bit 5V PCI bus
- 32-CH 5 V/TTL digital inputs/outputs
- 20 MHz (80 MBytes/s) maximum transfer rate
- 8, 16, or 32-bit transfers
- 4 auxiliary DI & 4 auxiliary DO
- On-board 64 kB FIFO
- On-board programmable timer pacer clock
- Timed digital input sampling controlled by Internal timer or external clock
- Independent trigger signals to start data acquisition and pattern generation
- Scatter-gather DMA
- Supports handshaking digital I/O transfer mode
- Repeated digital pattern generation from FIFO
- Active terminators for high speed and long distance data transfer
- Compact, half size PCB

Operating Systems
- Windows 2000/NT/XP/9x
- DOS
- Red Hat Linux
- Windows CE (call for availability)

Recommended Software
- VB/VC++/BCB/Delphi
- DAQBench

Driver Support
- PCIS-DASK for Windows 2000/NT/XP/9x
- PCIS-DASK/X for Red Hat Linux
- PCIS-OCX ActiveX controls
- PCIS-LVIEW/PnP ***NEW!***

Introduction

ADLINK PCI-7300A is an ultra-high speed digital I/O card. It consists of 32 digital input and/or output channel. High performance designs and state-of-the-art technology make this card ideal for a wide range of applications, such as high speed data transfer, digital pattern generation and digital pattern capture applications, and logic analyzer applications. Trigger signals are available to start the data acquisition of pattern generation.

Maximum Data Acquisition Rate

For sustained data transfer directly from or to host memory, could be 80MB/s. The maximum data transfer rates between external device and on-board FIFO can be up to 80MB/s for DO and 160MB/s for DI. 80MB/s is achieved by 32-bit bus width multiplied by internal 20MHz clock. 160MB/s is achieved by 32-bit bus width with external 40MHz clock for digital input channels only. The PCI-7300A can reach 160MB/s throughput only when the acquired data length is less than FIFO size (16 k samples).

Bus Mastering DMA

The PCI-7300A performs high-speed data transfers between on-board FIFO and host memory using bus mastering DMA and scatter gather via a 32-bit PCI bus architecture. PCI bus greatly extends data throughput up to 132 Mbytes/sec (burst) and also has provisions for processor-free DMA. When the PCI-7300A becomes the bus master, it takes control of the PCI bus, transfers data at burst speed, and then releases the bus. User can utilize the host memory as much as possible to store data when the data acquisition throughput is less than the sustained PCI bus bandwidth.

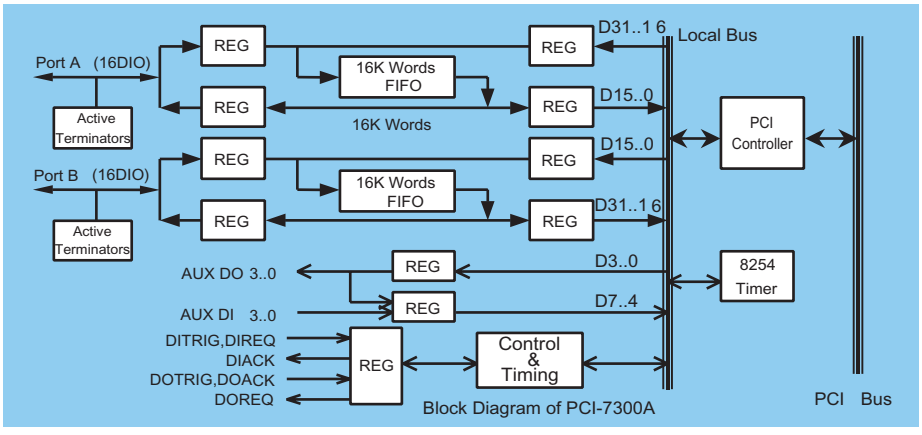
Scatter Gather Support

For bus master devices, the hardware has the special-design built-in support for transferring data to and from noncontiguous ranges of physical memory. The PCI-7300A contains multiple pairs of address and length registers, each one describing a single contiguous buffer segment. This allows PCI-7300A to perform I/O using buffers that are scattered throughout DMA address space. These multiple address and count registers are often referred to as a scatter/gather list, and you can also think of these bus masters as having their own built-in mapping registers. With scatter gather support, the data transfer size is no longer a limitation, and moreover, ring buffer is easily achieved with the link list of the scattered memory.

I/O Port Configurations

The PCI-7300A is initially configured as two ports, PORTA and PORTB. Each port controls 16 digital I/O lines. The I/O ports can be configured as either input or output. According to outside device environment, users can configure PCI-7300A to meet all high-speed digital I/O data transferring. PCI-7300A can support many different digital I/O operation modes:

- **Internal clock**
  The digital input and output operations are handled by internal clock and data is transferred by bus mastering DMA.
- **External clock**
  The digital input and output operations are handled by external In/Out strobe signals (DI_REQ or DO_ACK) and data is transferred by bus mastering DMA.
- **Handshaking**
  Through REQ and ACK signals, the digital I/O data can have simple handshaking data transfer to guarantee no data loss.
- **Pattern generation**
  The PCI-7300A reads or writes digital data at a predetermined rate. Users can control the rate internally by on-board counters with 50ns timing resolution.



Block Diagram of PCI-7300A